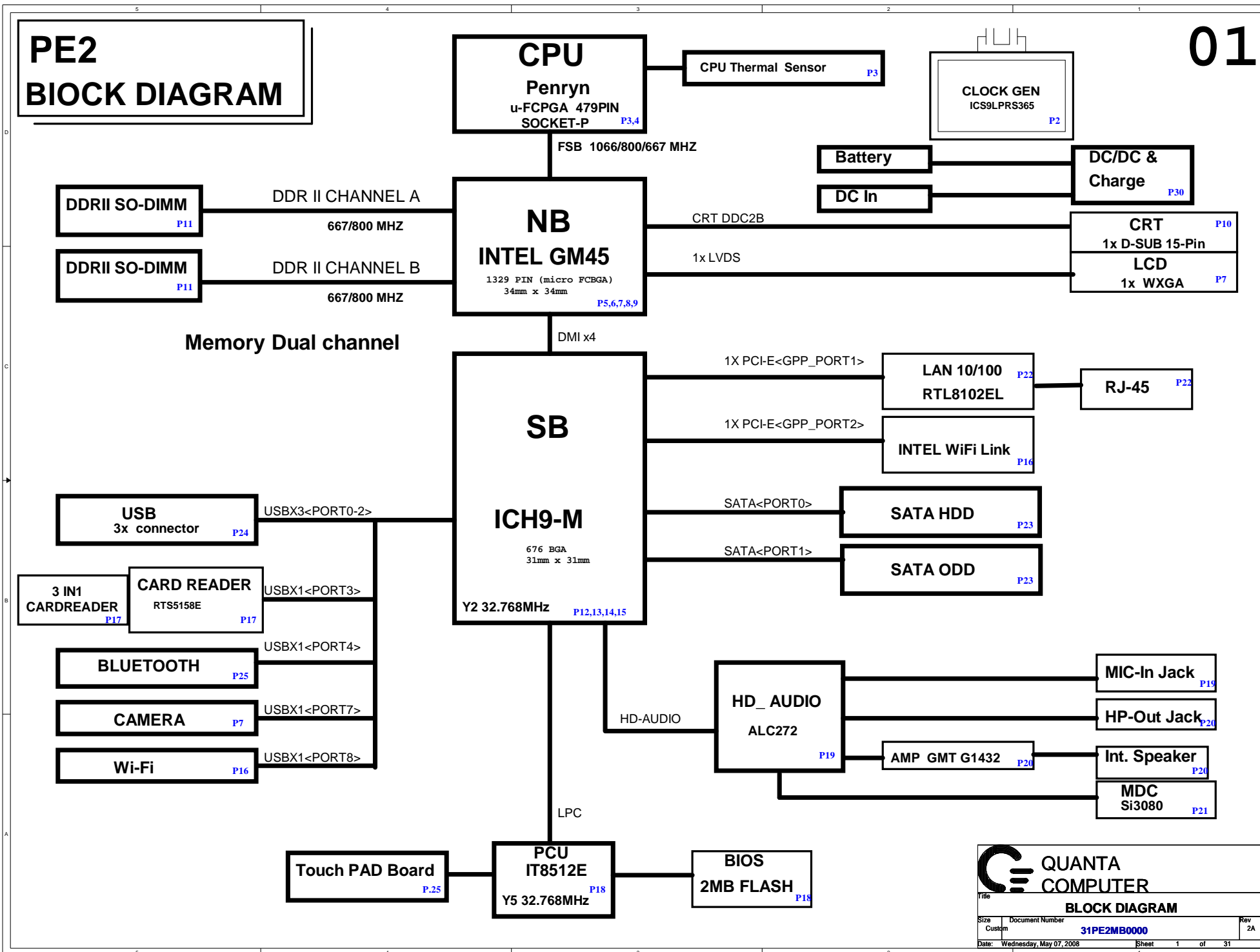


PE2 BLOCK DIAGRAM

01



[illegible]

27 Select PIN13	PIN 20/21	PIN 24/25
* 0	DOT_96 / DOT_96#	LCDCLK / LCDCLK#
1	SRC_0 / SRC_0#	27M / 27M_SS

Byte0 Bit4: iAMT Enable/Disable Control

ITP_EN(PIN14)	PIN53/54
* 0	SRC8/SRC8#
1	ITP/ITP#



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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466
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CLKGEN

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Document Number **PE2 MAIN BOARD**

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Wednesday

May 6

07, 2008

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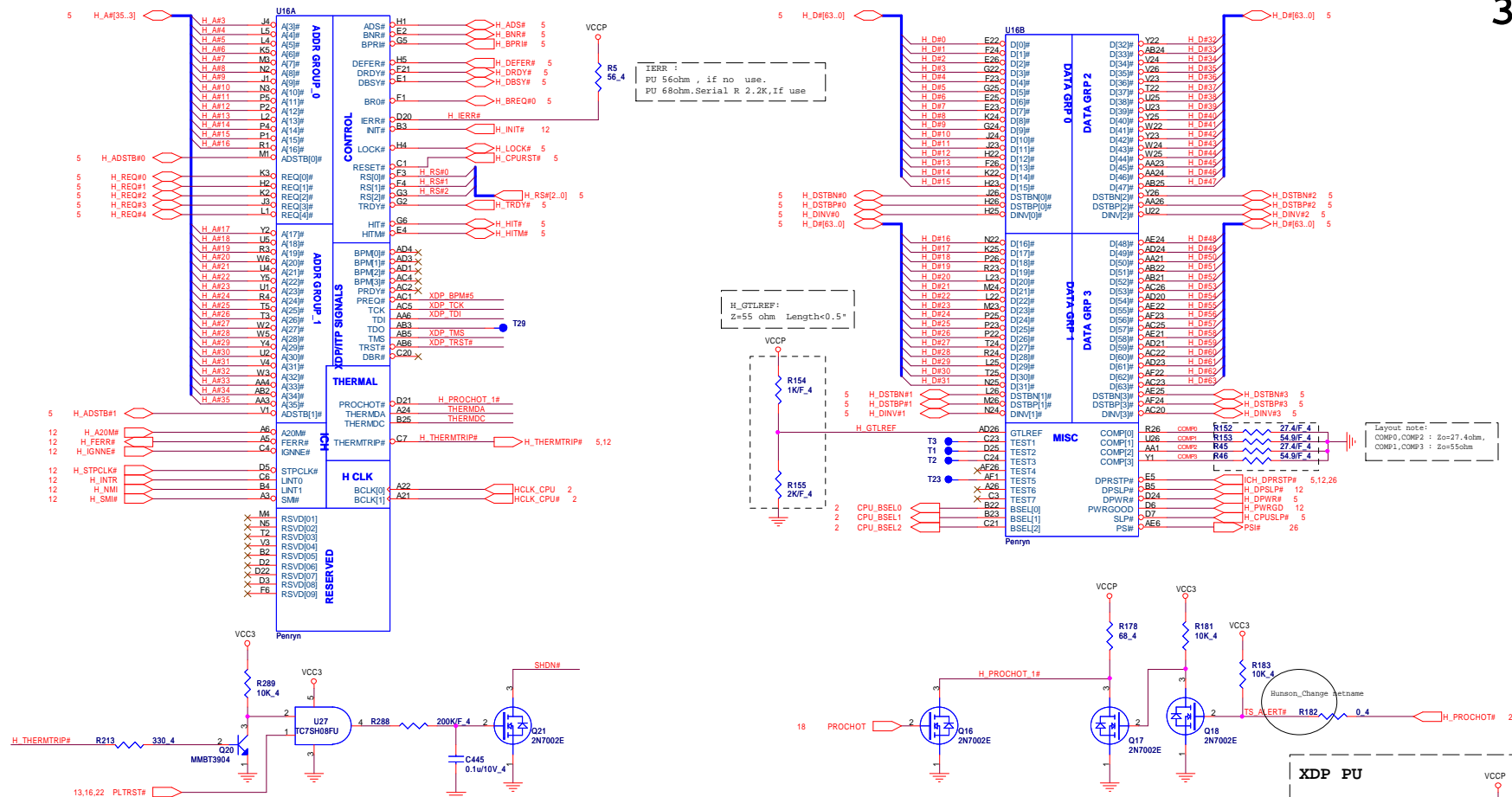
Sheet
5

of

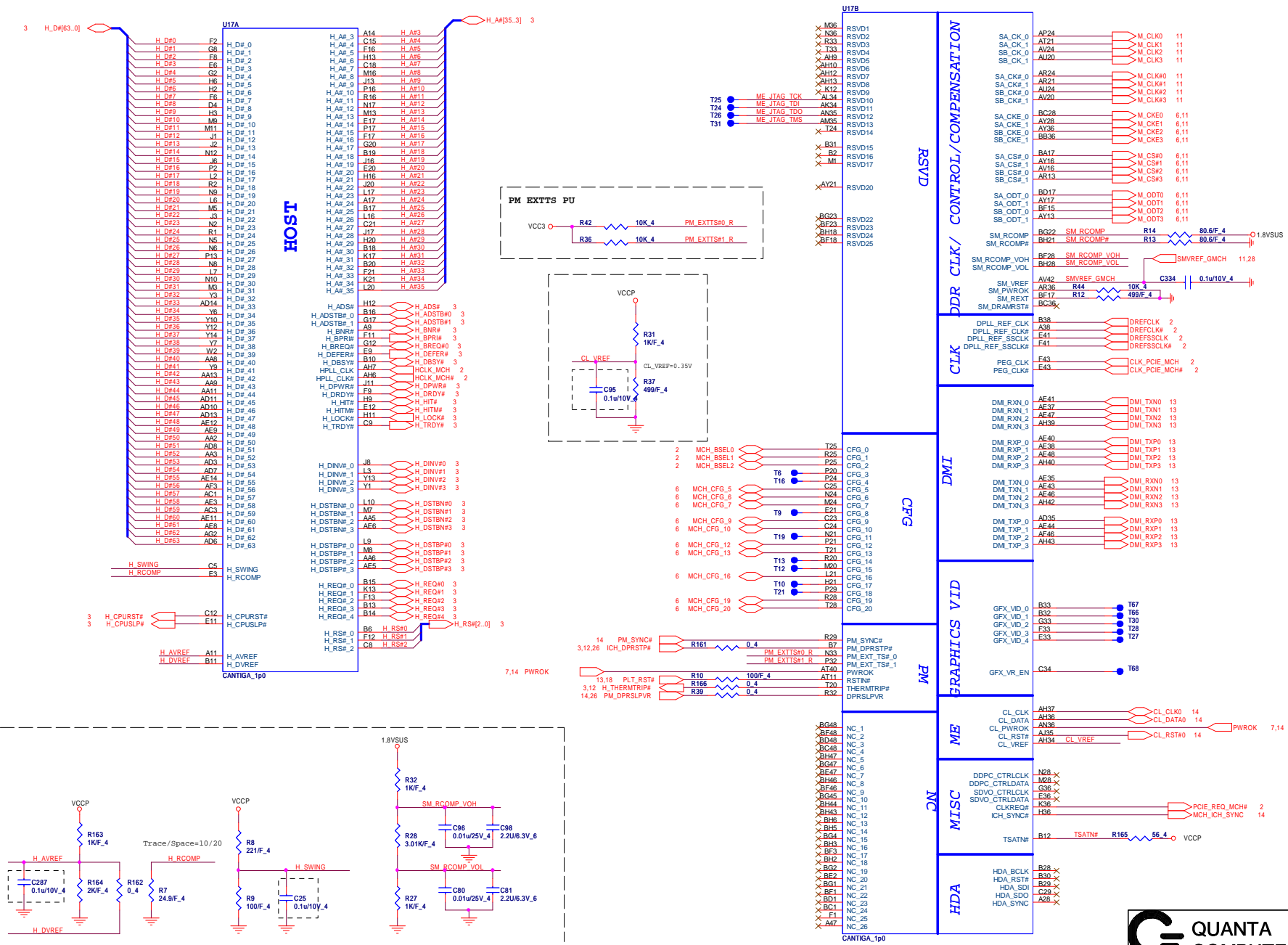
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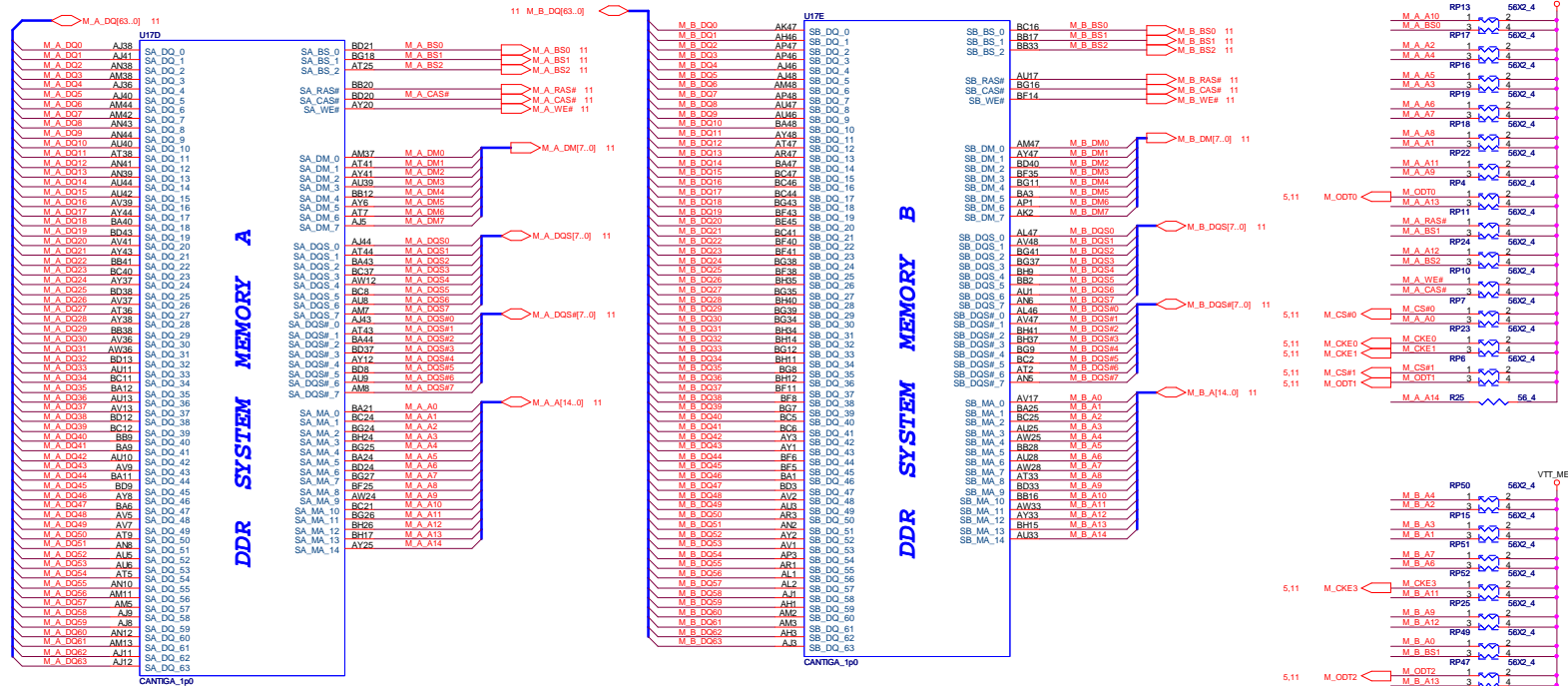
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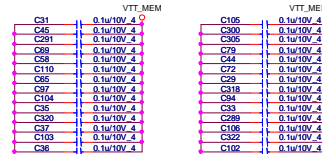


GMCH Strap pin description

	Low	High
c0p5	DM62	DM64
c0p6	TPM HOST interface enable	TPM HOST interface disable
c0p7	AMT Firmware will use TLS cipher suite with no confidentiality	AMT Firmware will use TLS cipher suite with confidentiality
c0p9	PCIe Graphics lan : Reverse Lane	PCIe Graphics lan : Normal operation
c0p10	PCIe Loopback enable	PCIe Loopback disable
c0p16	FSB Dynamic ODT Disabled	FSB Dynamic ODT Enabled
c0p19	DMI LANE Normal	DMI LANE Reversed
c0p20	only SDVOIP/HDMI or PCIe is operational	SDVOIP/HDMI and PCIe are operation simultaneously via the PEG port
c0p[12:13]	rx0r / ALLZ / Clock Un-gating	
	00 = Reserve	
	01 = XOR mode enabled	
	10 = All-Z mode enabled	
	* 11 = Normal Operation(Default)	

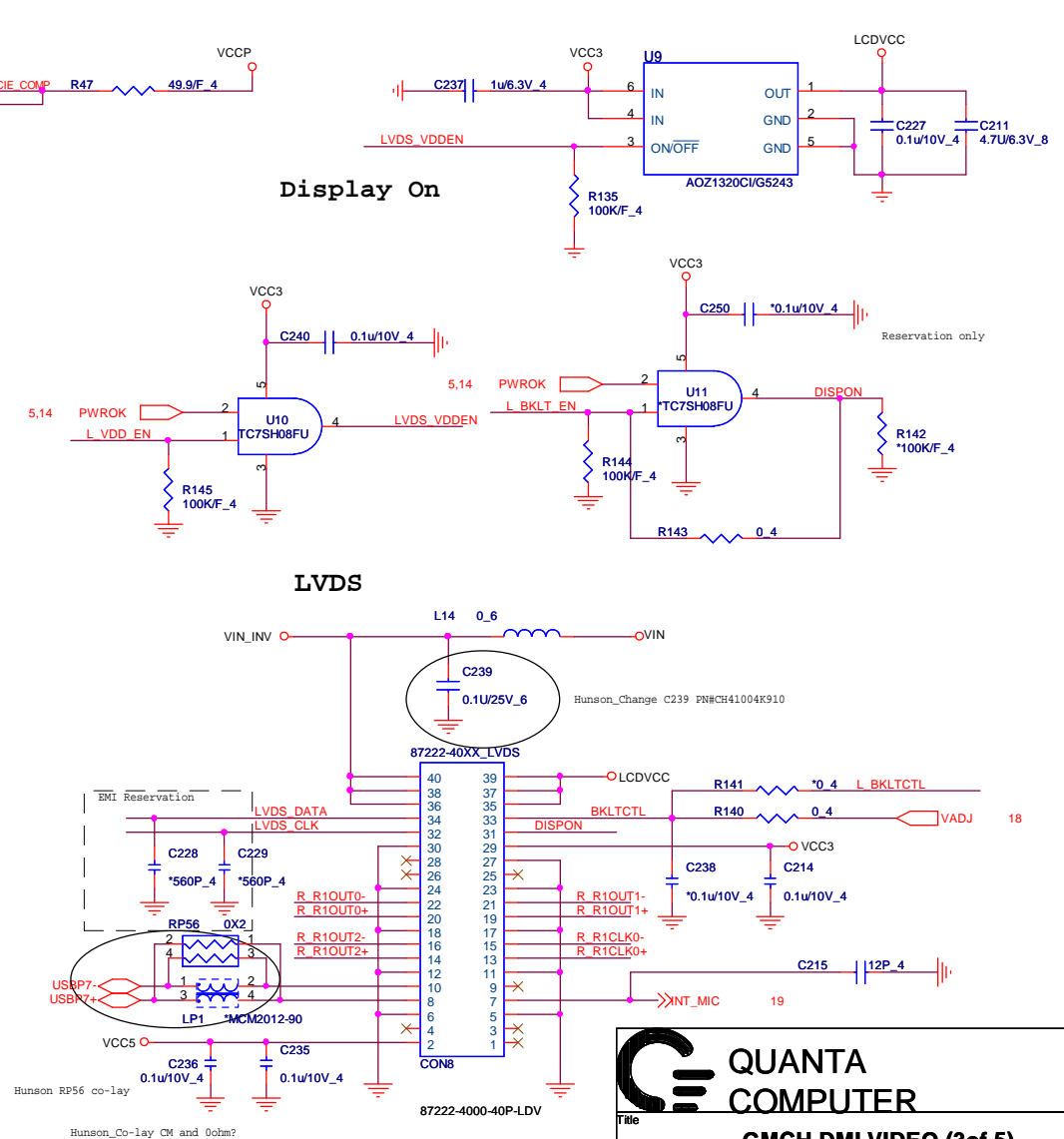
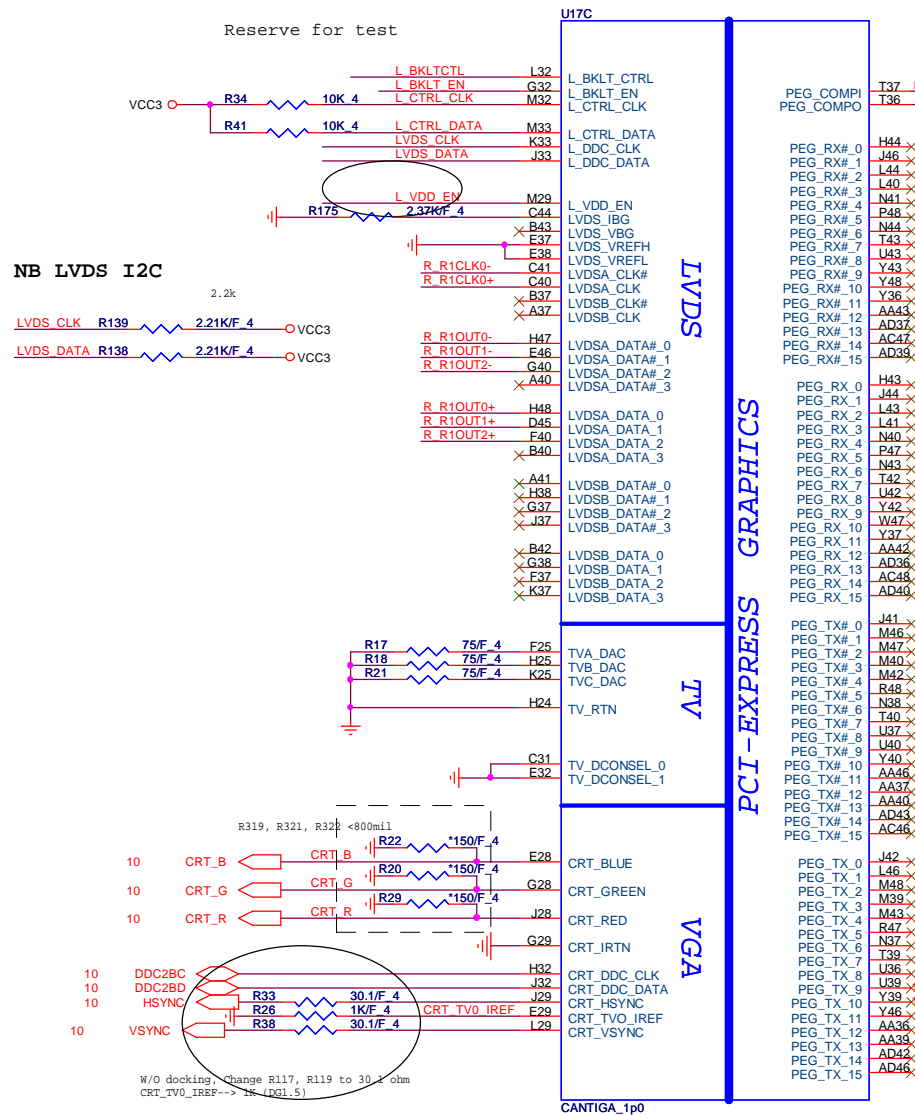
Int.Pull-down : CFG 18,19,20

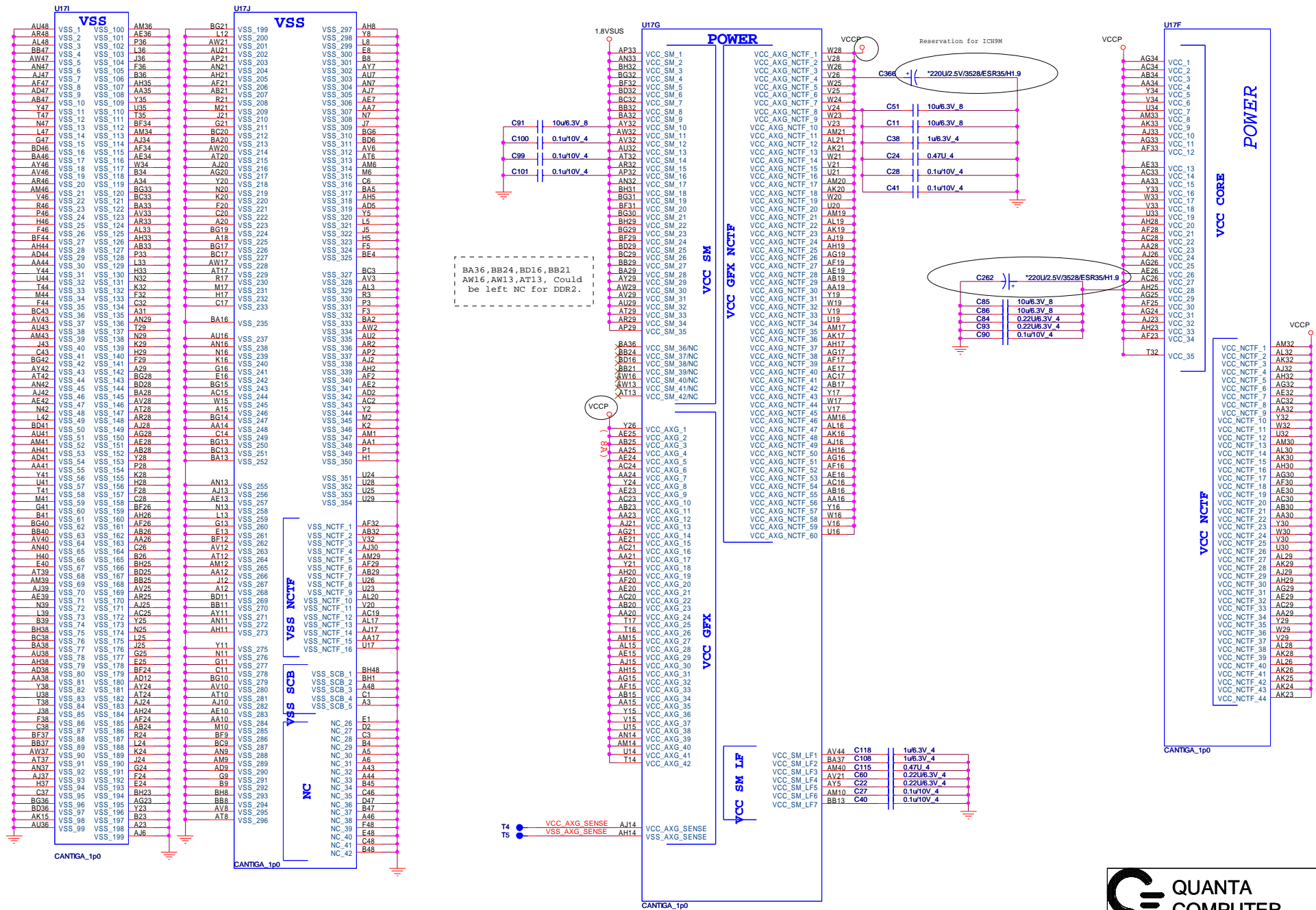
Int.Pull-high : CFG CFG 3-17



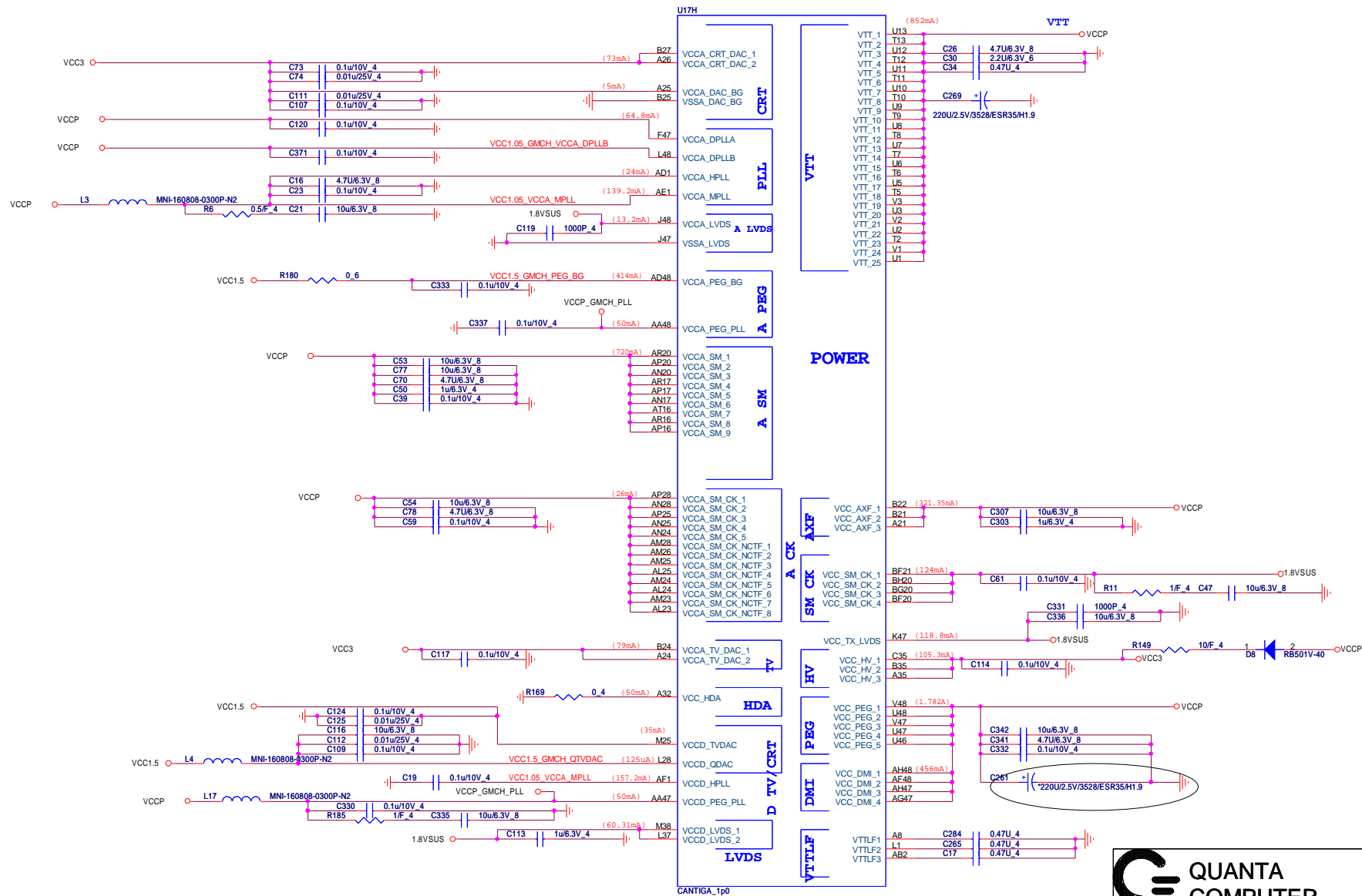
LVDS enable

7

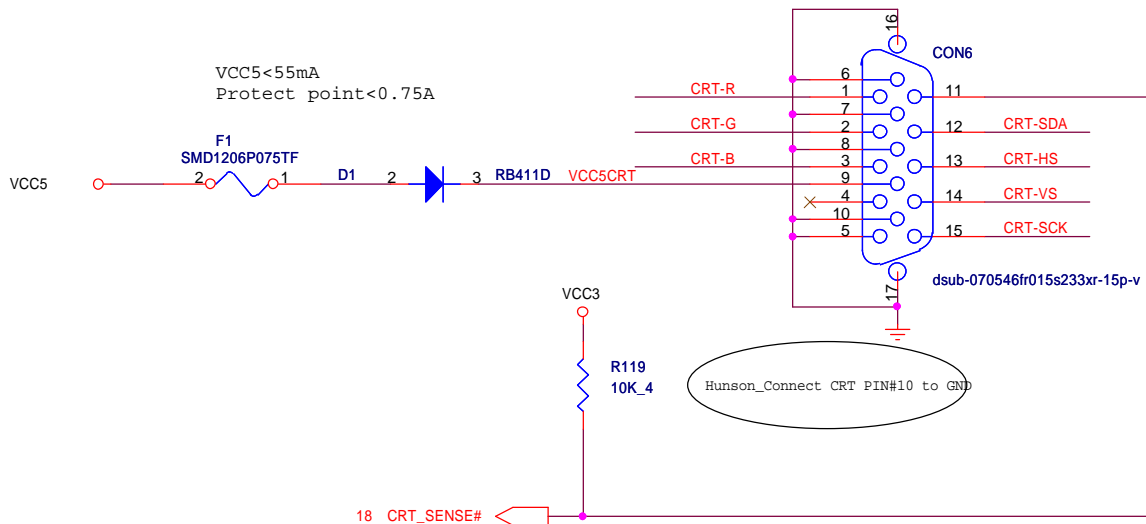
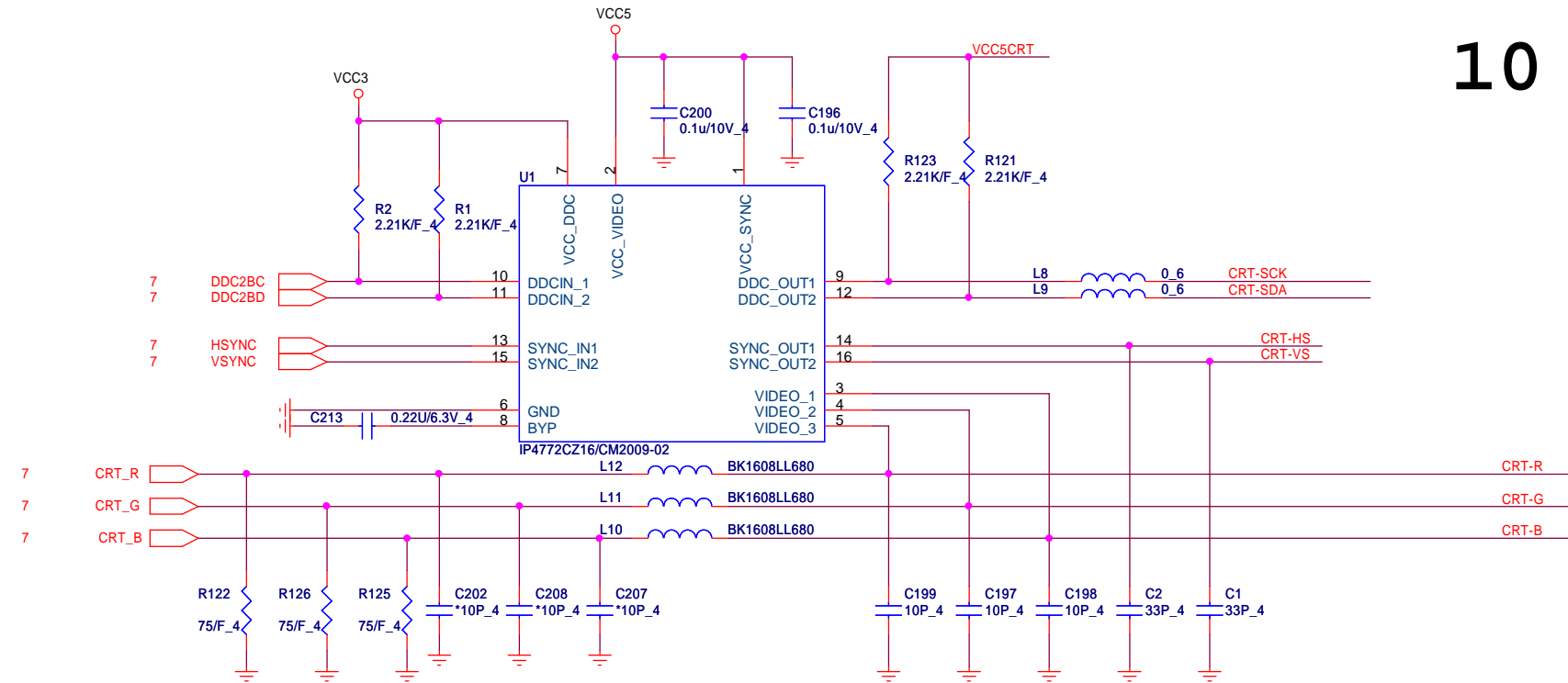




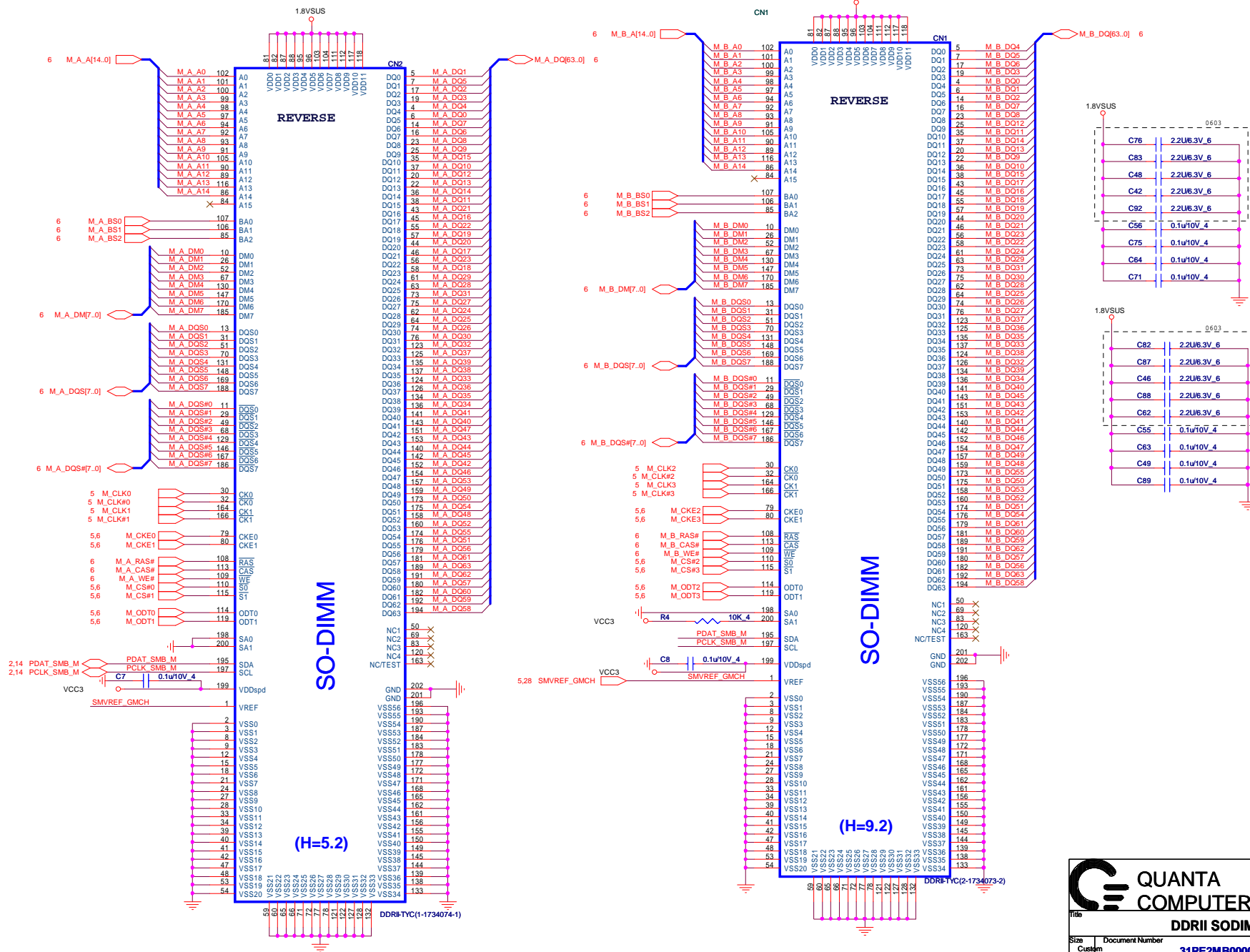
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COMPUTER

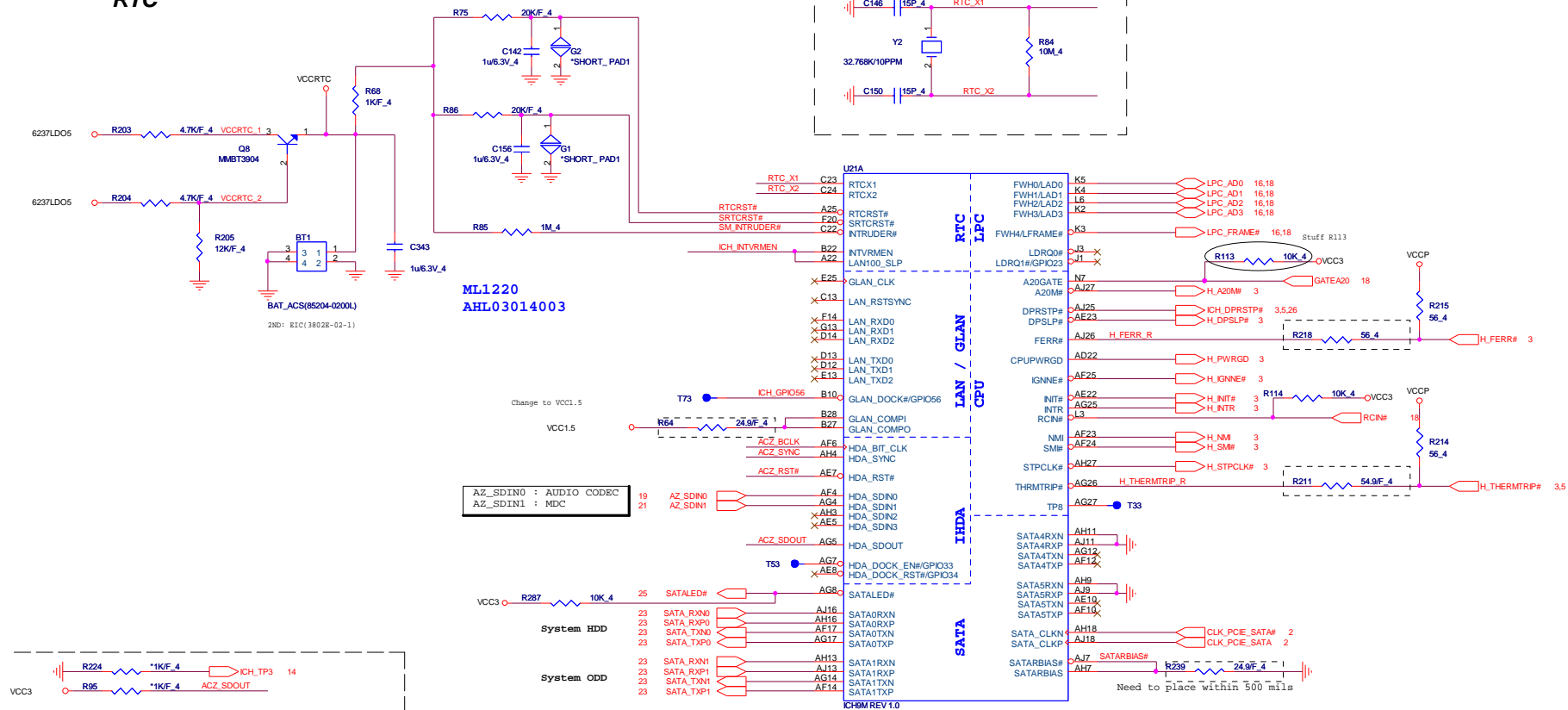


10



Title			CRT	
Size	Document Number	Rev		2A
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Date:	Wednesday, May 07, 2008	Sheet	10	of 31





ICH_TP3	ACZ_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	* Normal operation
1	1	Set PCIe port config bit 1

	INTVRMEN
Enable (default)	1
Disable	0

Hunson_Change PN#CS43322PB15 (0402 SIZE)

Hunson_Change R240, R241 to 68 ohm from 33ohm?
Check with EMI



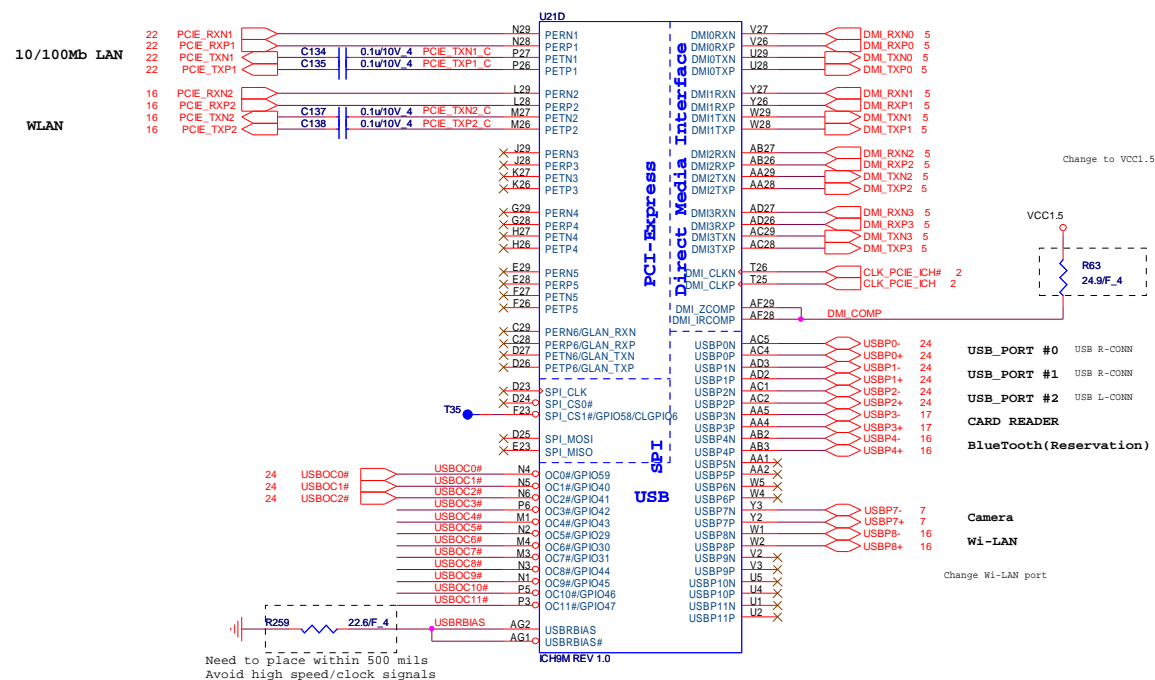
Title **ICH9-M HOST(1 of 4)**

Size	Document Number
Custom	31PE2MB0000

Date: Wednesday, May 07, 2008

Sheet 12 of 31

	Rev
	2



GPIO49 : NC
GPIO20 : Can't pull high.

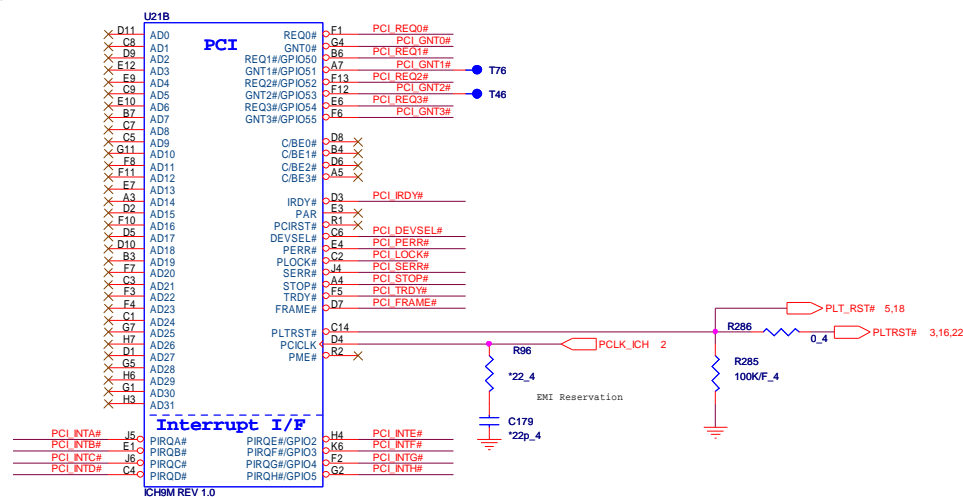
A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default
-----------	---

ICH9 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	PCI (Default)

IRQ	Description
PIRQA	USB UHCI Controller #1,USB UHCI Controller #4
PIRQB	Audio, Modem, SMI/Bus
PIRQC	USB UHCI Controller #3,SATA/IDE Native Mode
PIRQD	USB UHCI Controller #2
PIRQE	NT LAN: option for SC ₁ TC ₀ HPeT #0,1,2; R5C847
PIRQF	option for SC ₁ TC ₀ HPeT #0,1,2 R5C847
PIRQG	option for SC ₁ TC ₀ HPeT #0,1,2 R5C847
PIRQH	USB EHCI Controller:option for SC ₁ TC ₀ HPeT #0,1,2



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11

ICH9-M PCI-E, USB, PCI (2 of 4)

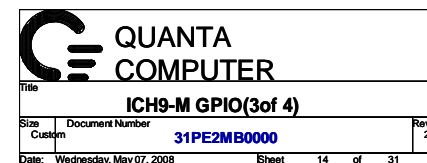
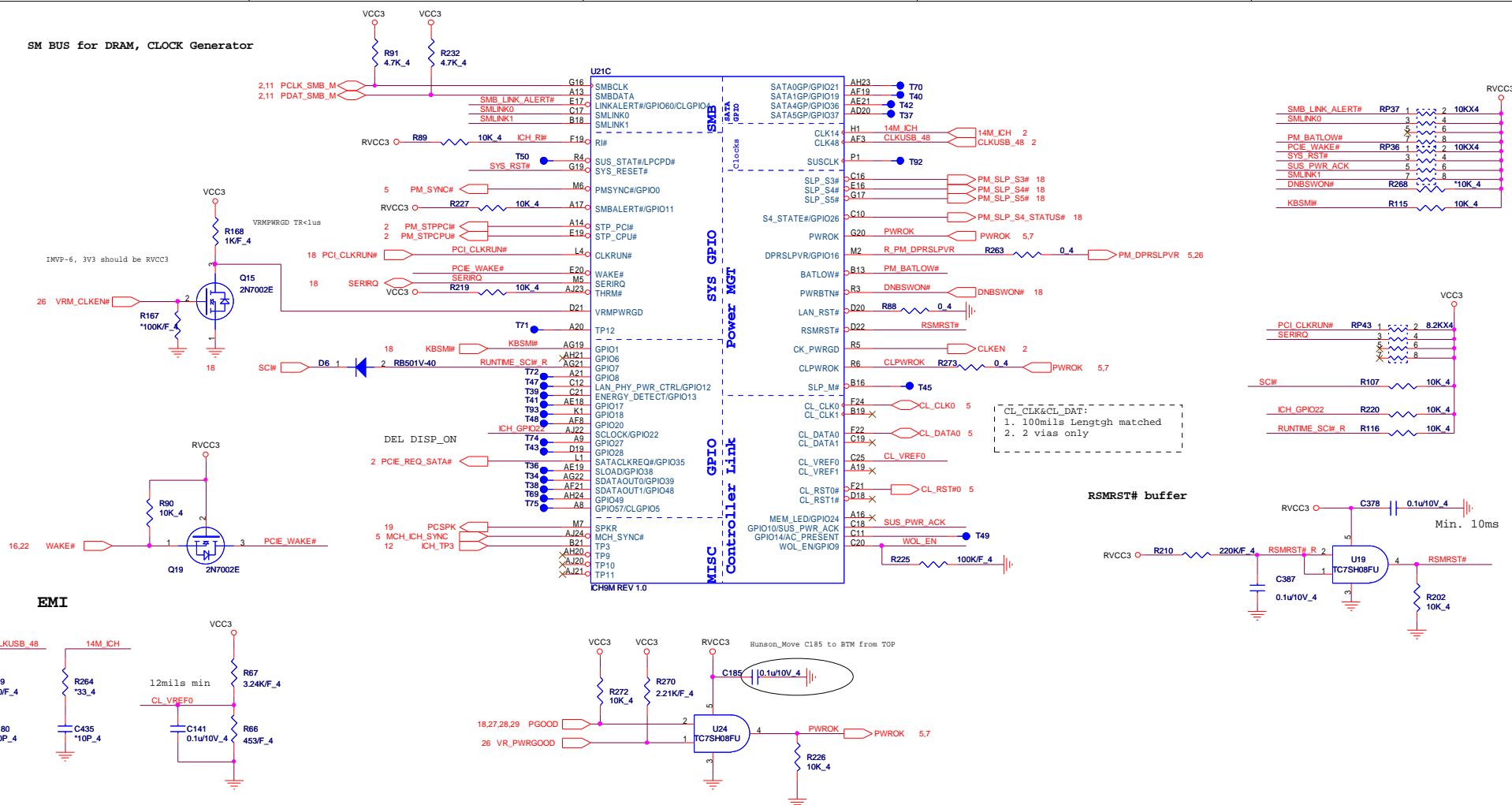
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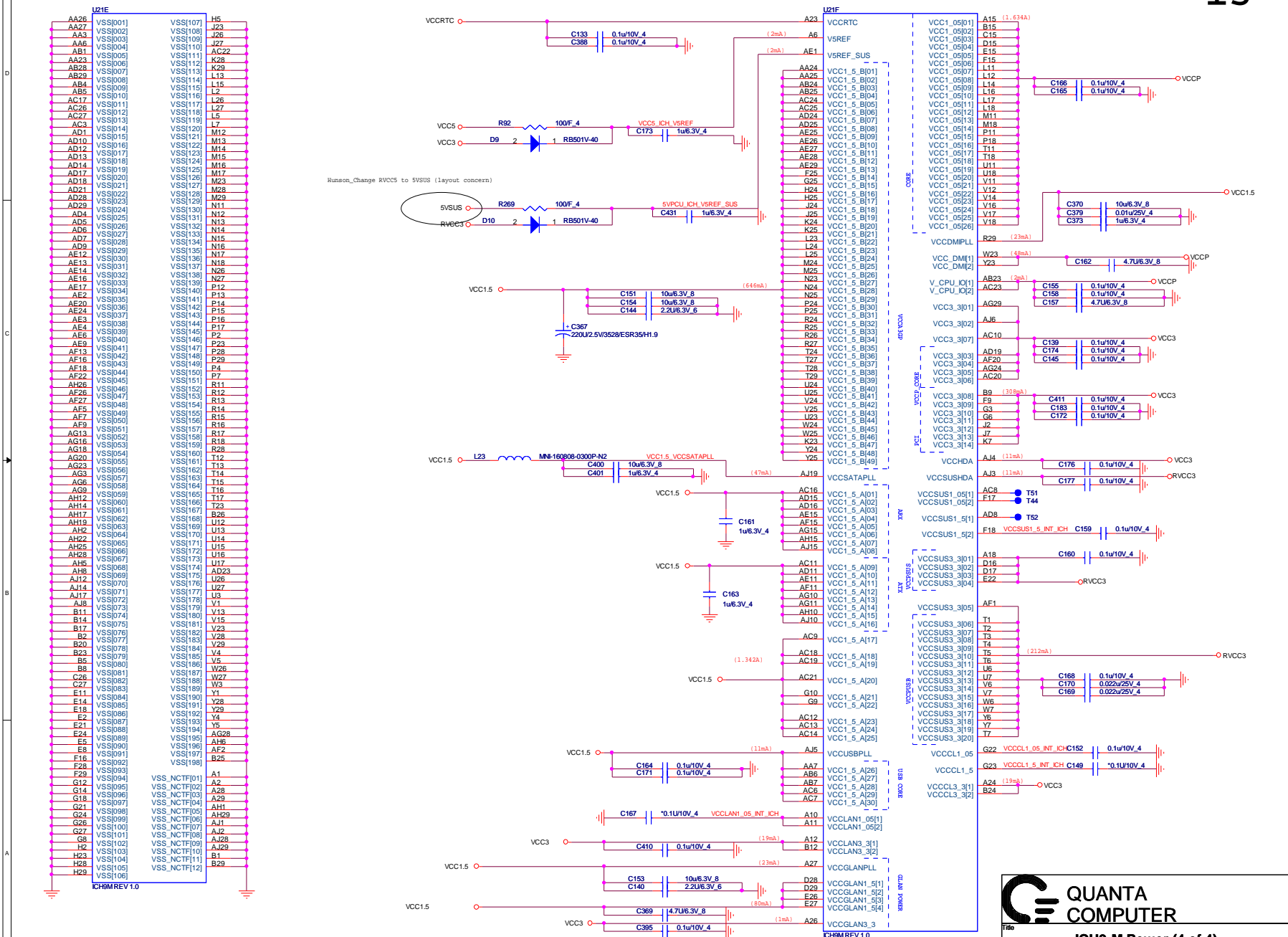
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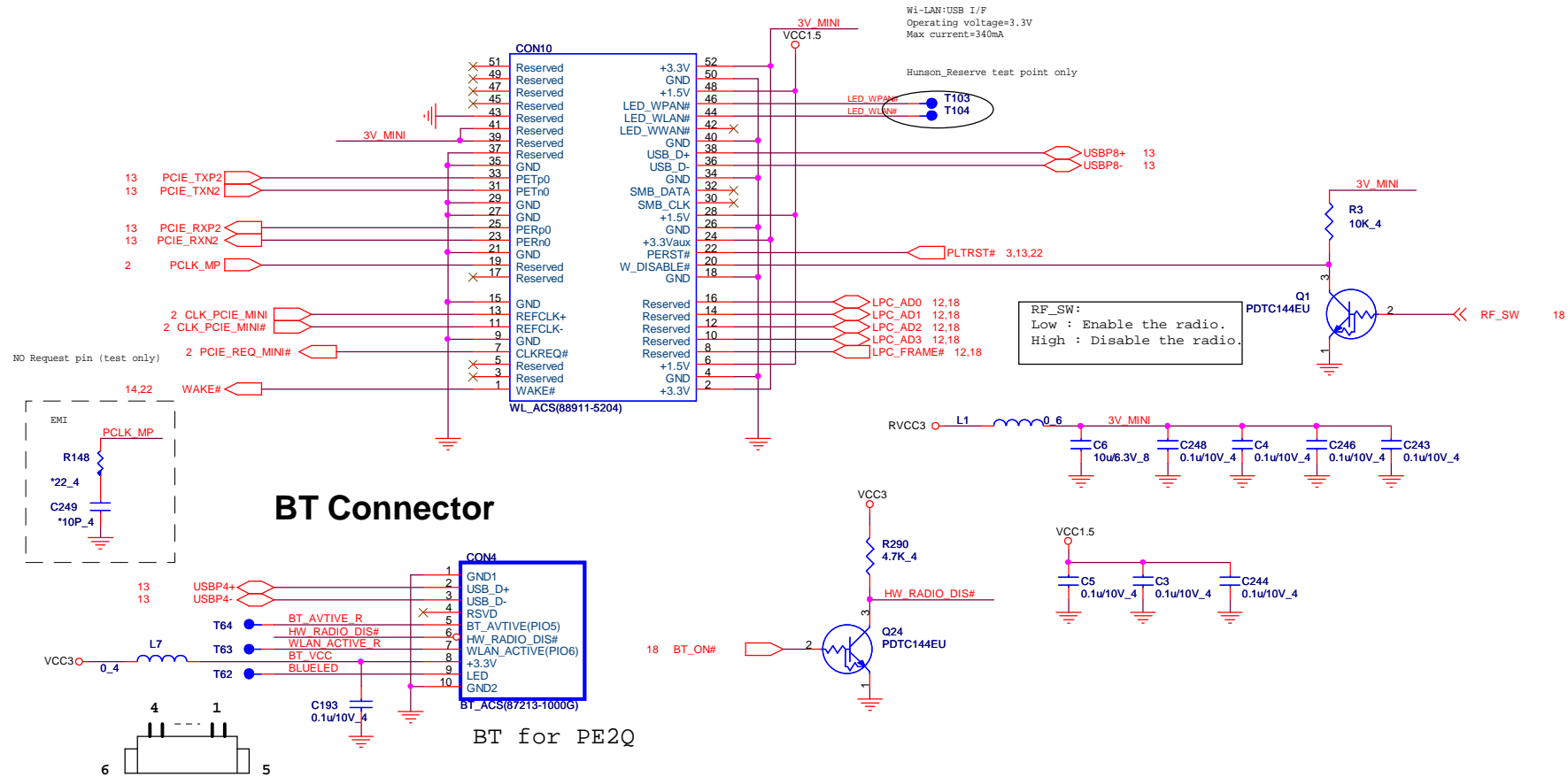
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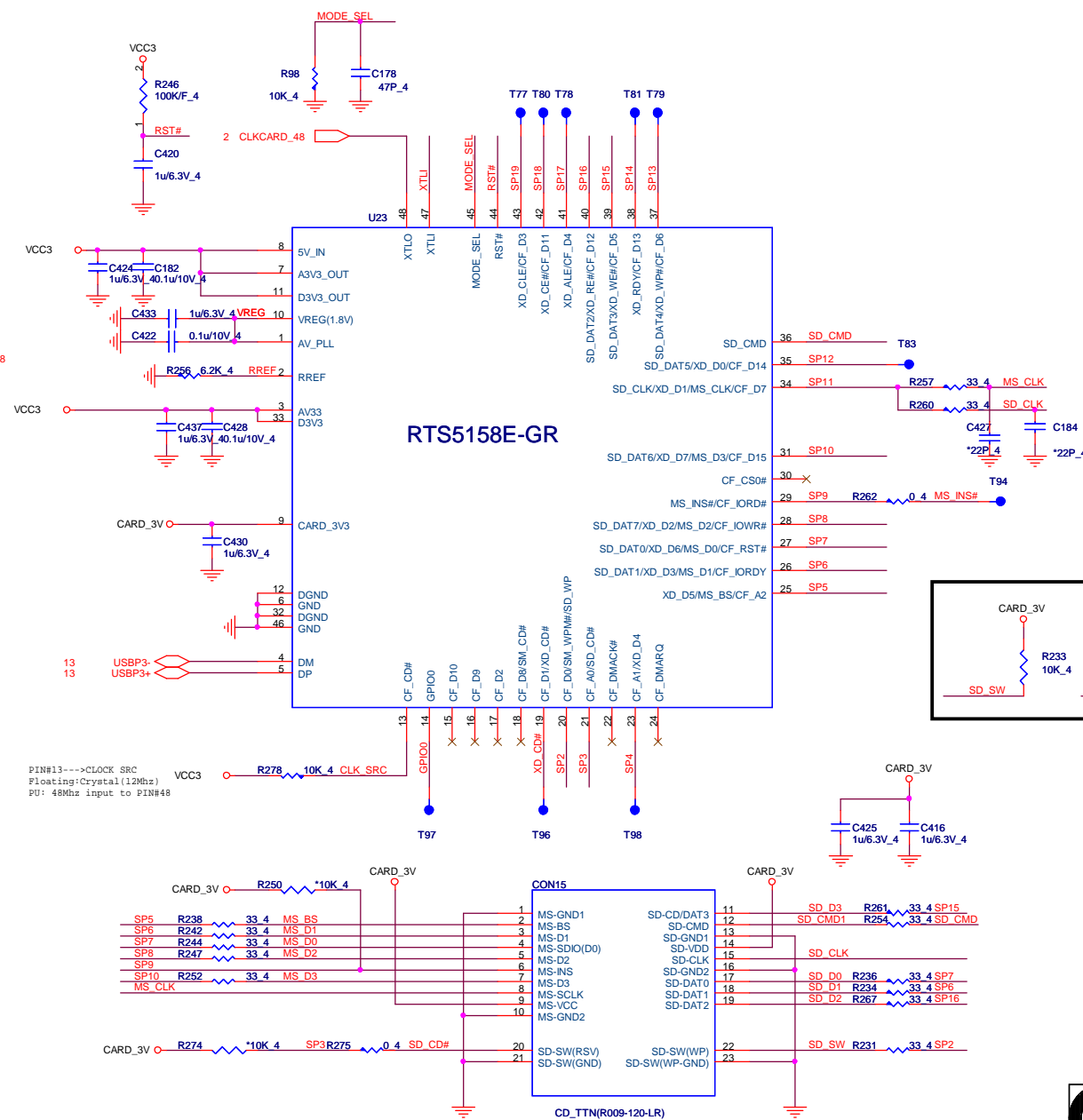
Rev





Mini PCI-E Card--W-LAN





2ND:MLX(47265-0001)

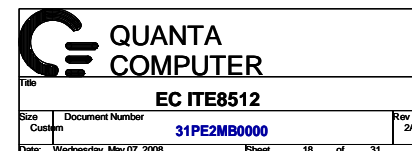
Supporting MMC/SD/MS Cards



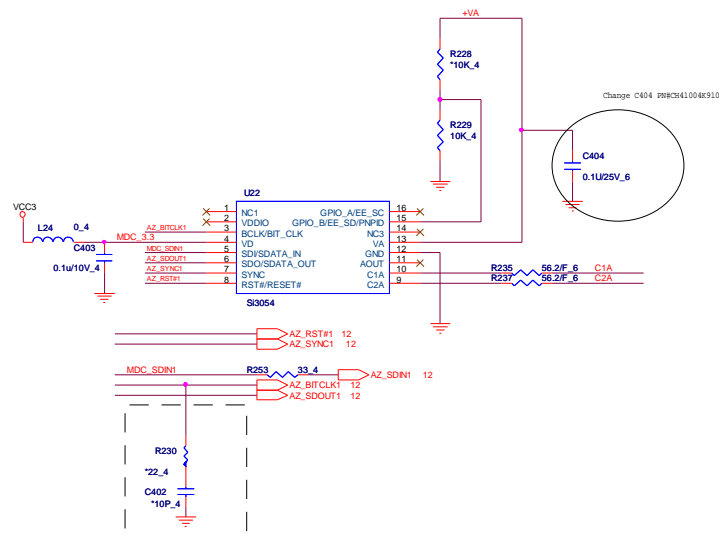
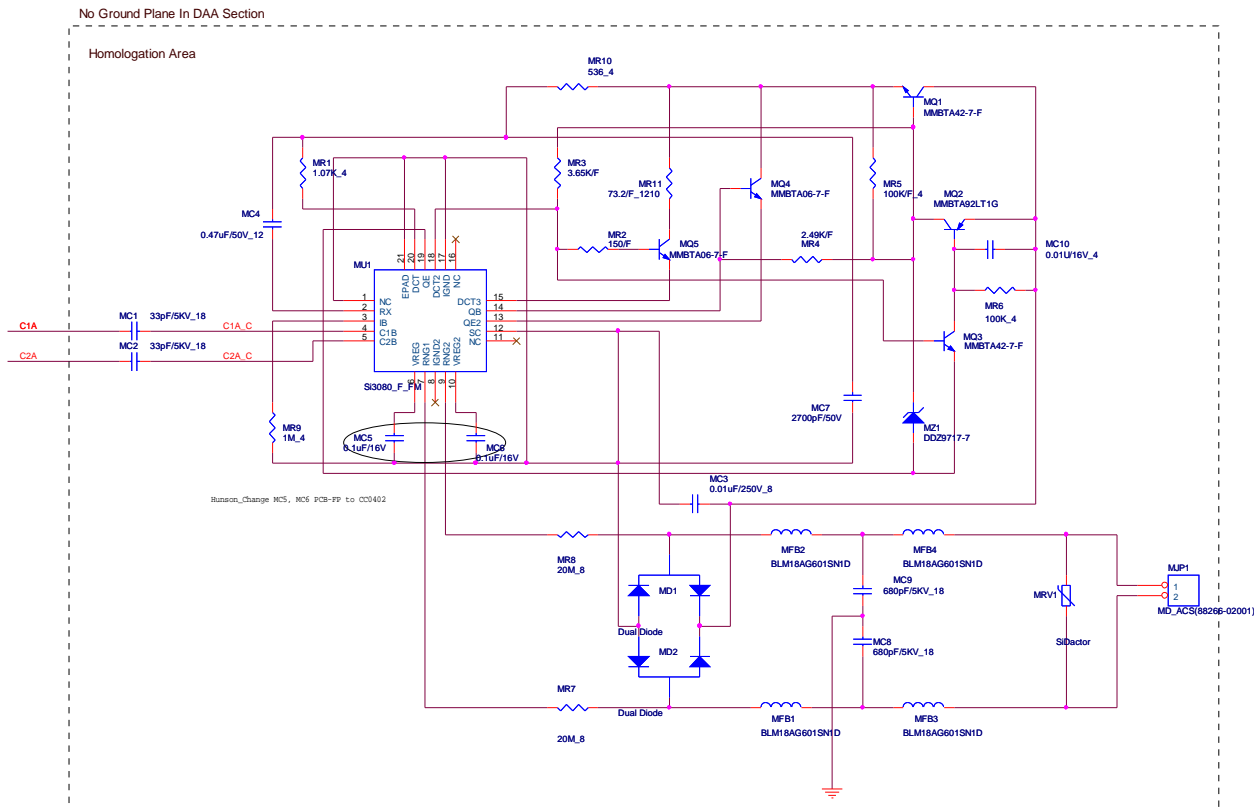
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RST5158 & 3 in 1

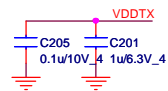
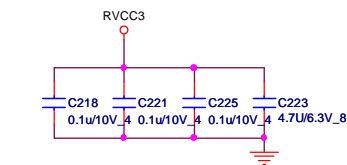
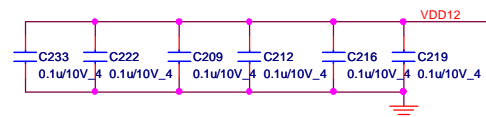
Size Custom	Document Number 31PE2MB0000	Rev 2A
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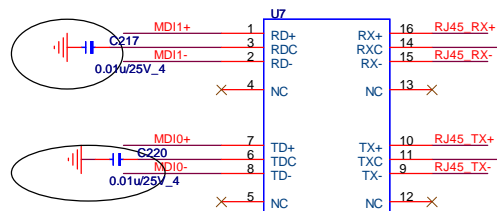




22

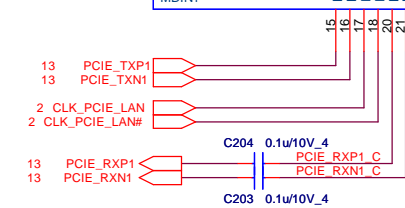
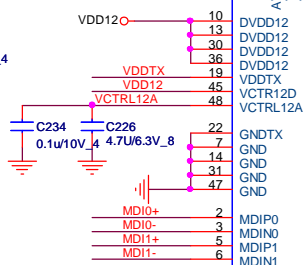
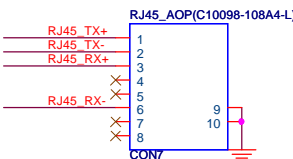


Hunson Change C217, C220 to CH31004KB17 (0.01uF)

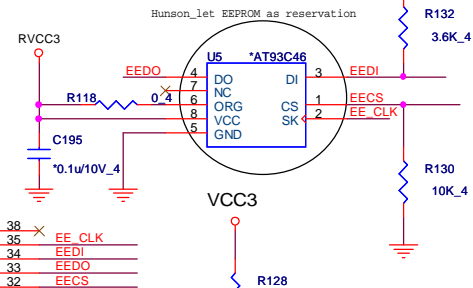


NS681686
LF-H49P-16P-LDH

RJ45

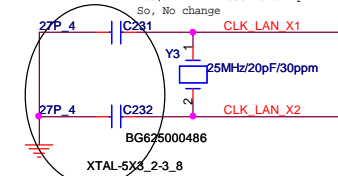


RTL8102EL-VB-GR



Hunson let EEPROM as reservation

Hunson_Change to 33p from 27pF based tuning
But, RTL FAE recommend 27pF
So, No change

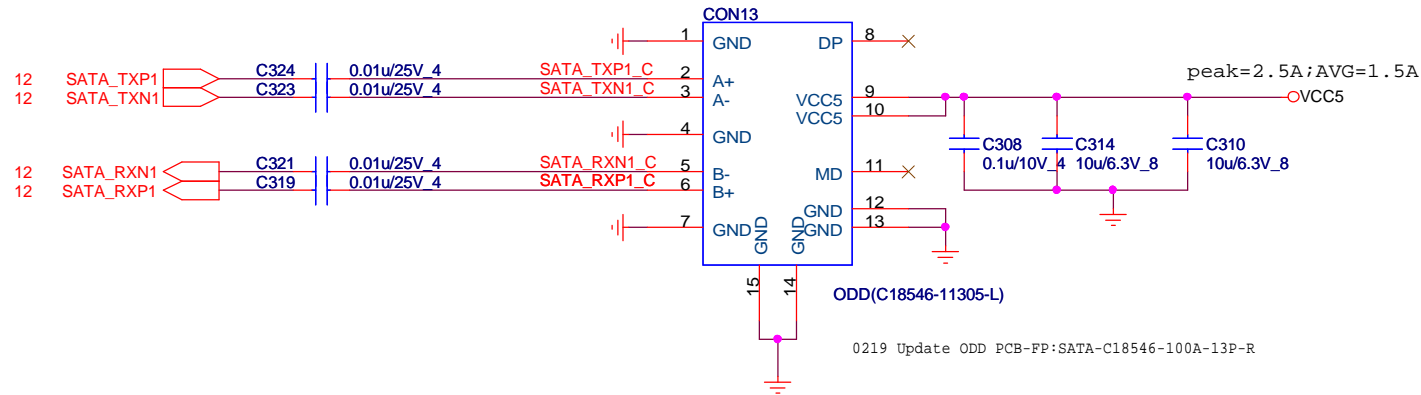


XTAL-5X3-2-3-8

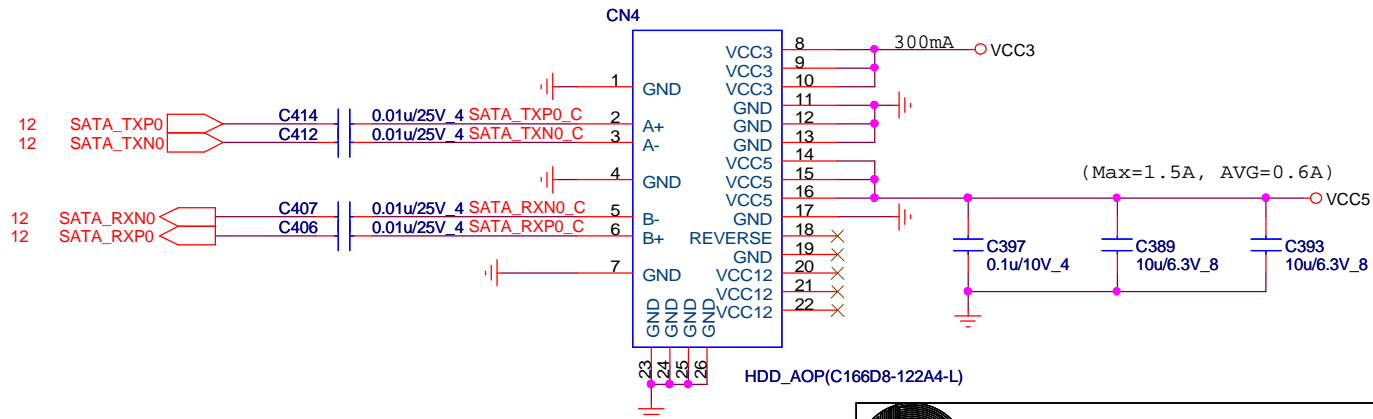
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Title LAN RTL8102EL			
Size Custom	Document Number 31PE2MB0000		Rev 2A
Date: Wednesday, May 07, 2008	Sheet 22 of 31		

ODD CONNECTOR

23



HDD CONNECTOR



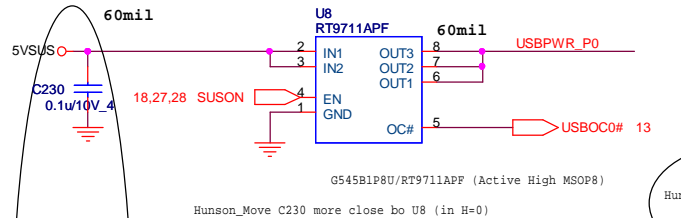
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Title		
HDD, ODD		
Size	Document Number	Rev
Custom	31PE2MB0000	2A
Date: Wednesday, May 07, 2008		
Sheet 23 of 31		

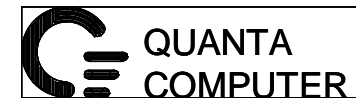
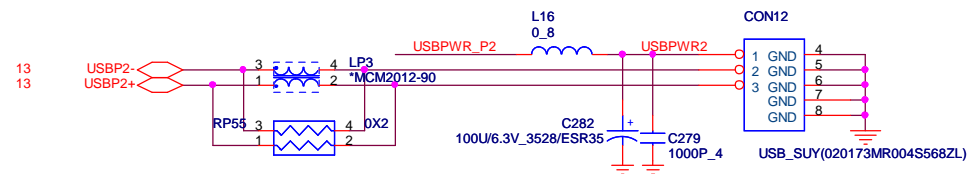
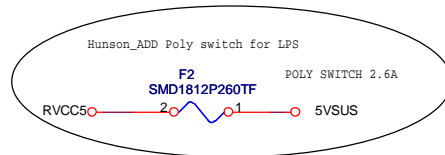
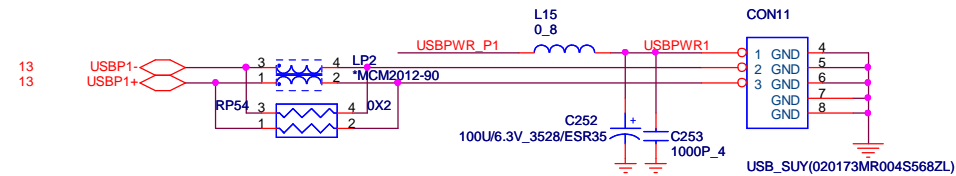
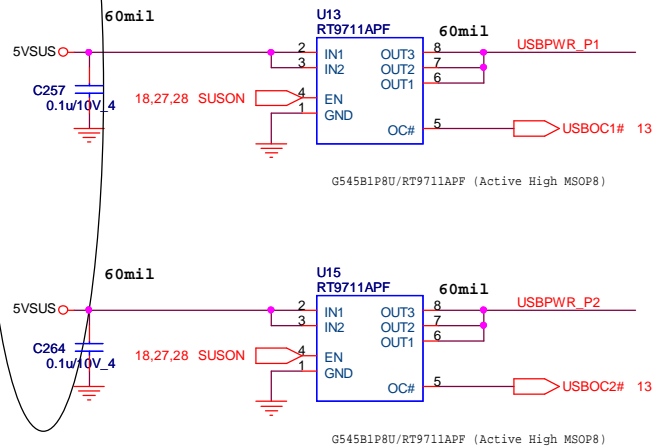
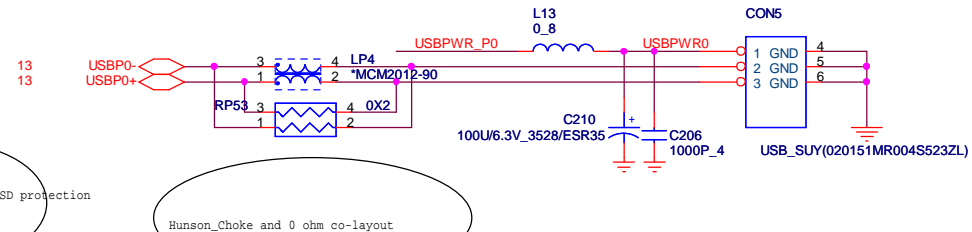
USB Connector

USB Power and Over current

Change from RVCC5 to 5VSUS



Hunson_Remove USB ESD protection



Title
USB x3

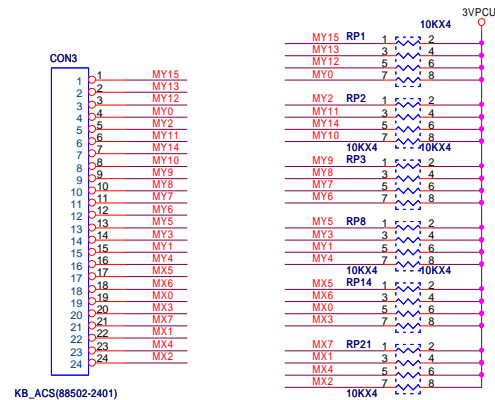
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Custom **31PE2MB0000**

Date: Wednesday, May 07, 2008

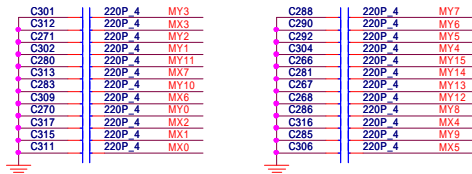
Sheet 24 of 31

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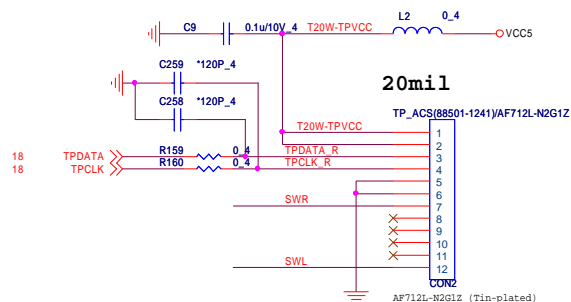
INT. KEYBOARD



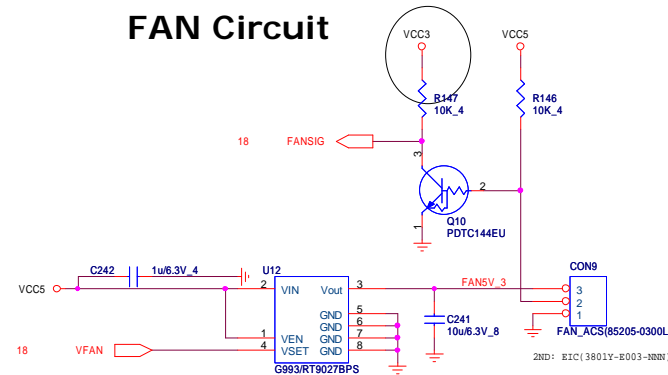
MX[0..7] >> MX[0..7] 18
 MY[0..15] >> MY[0..15] 18



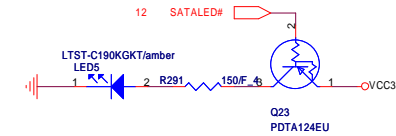
TOUCHPAD BOARD CON



FAN Circuit



HDD LED



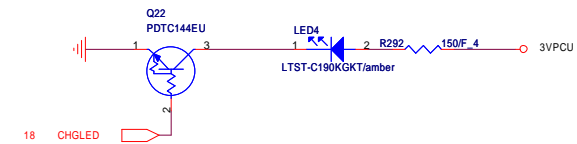
POWER STATUS LED

Power LED-->Low Active



CHARGE LED-->High Active

BATTERY CHARGE LED



Wi-Fi CHARGE LED



Hunson_Wake on WLAN not supported

NumLED

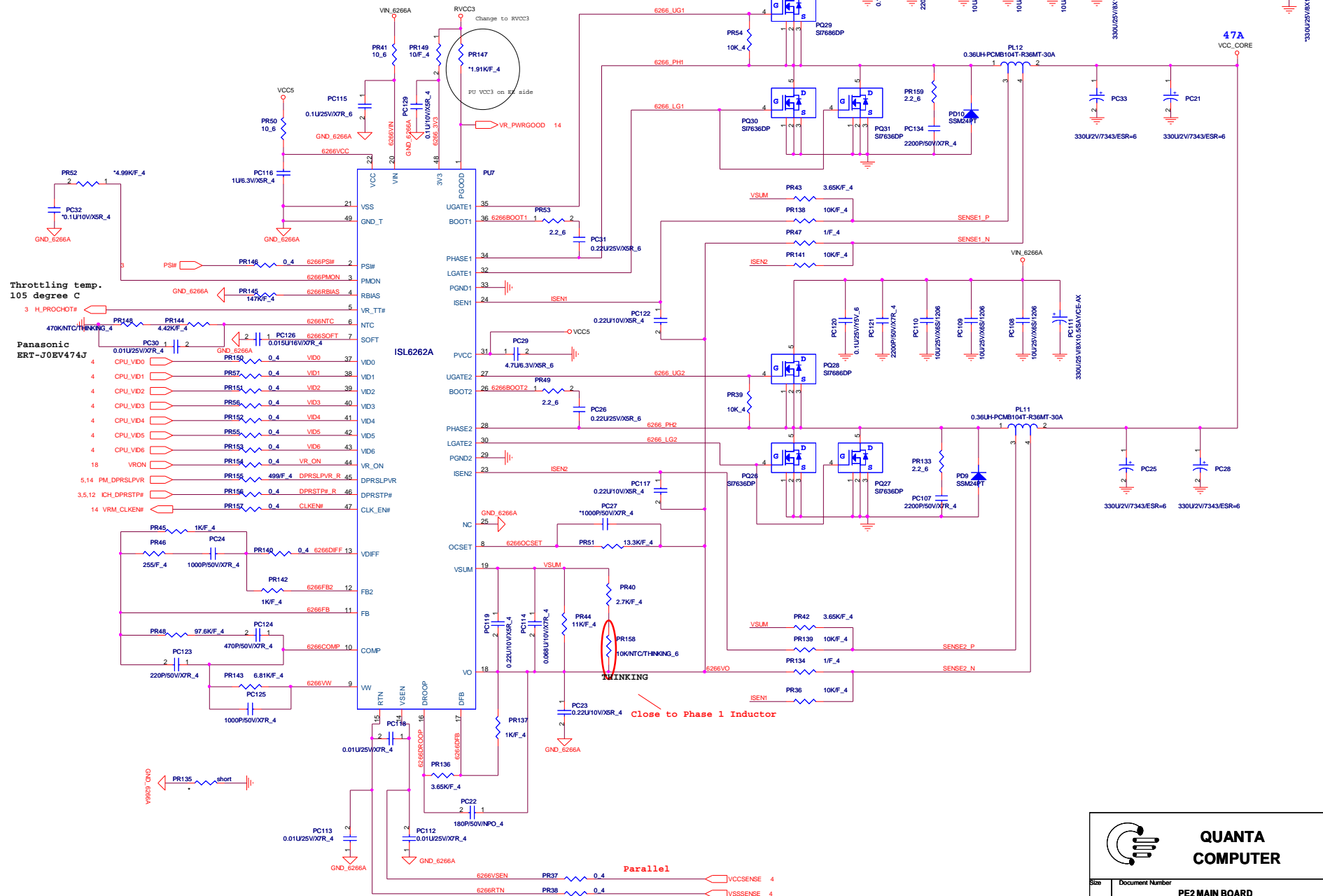


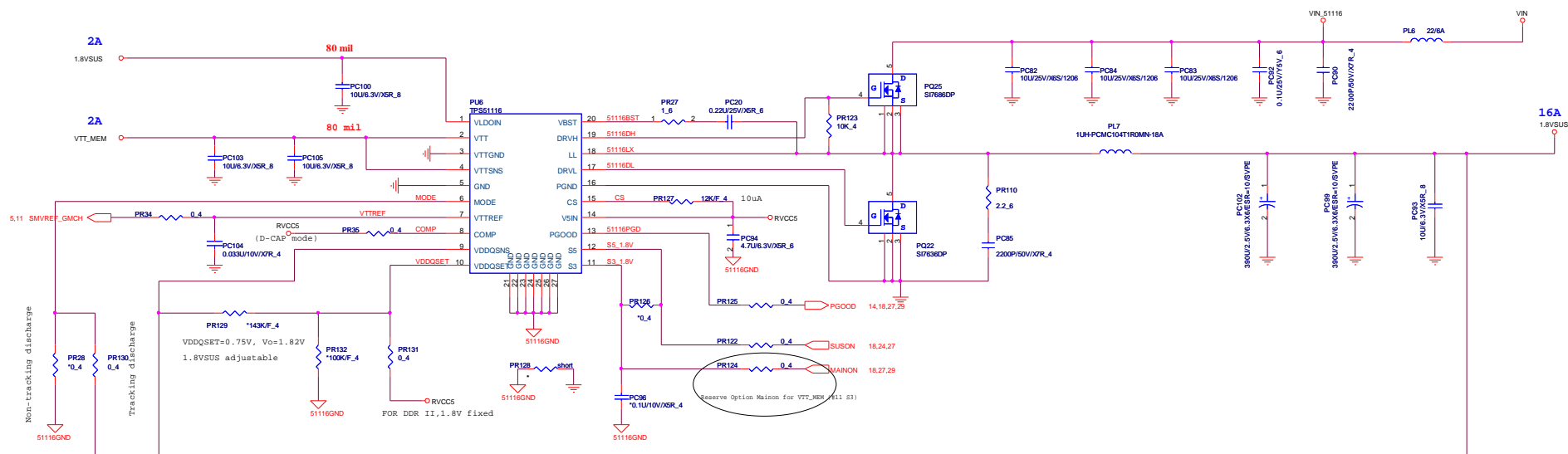
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File: **K/B, FAN, LED, T/P**

Size: Custom Document Number: **31PE2MB0000**

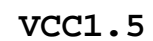
Date: Wednesday, May 07, 2008 Sheet 25 of 31





VDDQSET	VDDQ(V)	VTTREF & VTT	NOTE
GND	2.5 fixed	VDDQSNS/2	DDR
5V	1.8 fixed	VDDQSNS/2	DDR2
FB-Resistor	Adjustable	VDDQSNS/2	1.5V<VDDQ<3V

STATE	S3	S5	1.8VSUS	VTTREF	VTT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off



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